AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A semiconductor package comprising:

a plurality of leads, each of the leads defining:

a generally planar first surface;

a generally planar second surface disposed in opposed relation to the first surface; and

a generally planar third surface disposed in opposed, substantially parallel relation to the second surface and laterally offset outwardly relative to the first surface;

a first semiconductor die defining opposed top and bottom surface;

a second semiconductor die defining opposed top and bottom surfaces;

a plurality of conductive connectors electrically and mechanically connecting the first semiconductor die to the first surfaces of the leads and the second semiconductor die to the second surfaces of the leads; and

an encapsulating portion applied to and at least partially encapsulating the leads, the first and second semiconductor dies, and the conductive connectors such that at least the first and second surfaces of each of the leads are covered by the encapsulating portion.

2. (Original) The semiconductor package of Claim 1 wherein the conductive connectors each comprise a conductive bump.

3. (Original) The semiconductor package of Claim 2 wherein the conductive bump is fabricated from material selected from the group consisting of:

gold; and

solder.

4. (Original) The semiconductor package of Claim 1 wherein:

the first semiconductor die includes a plurality of bond pads disposed on the top surface thereof;

the second semiconductor die includes a plurality of bond pads disposed on the bottom surface thereof; and

the conductive connectors are used to electrically and mechanically connect the bond pads of the first semiconductor die to respective ones of the first surfaces of the leads and the bond pads of the second semiconductor die to respective ones of the second surfaces of the leads.

5. (Original) The semiconductor package of Claim 4 wherein the conductive connectors each comprise a conductive bump.

6. (Original) The semiconductor package of Claim 1 wherein:

each of the leads includes a first bump land formed at a prescribed region of the first surface thereof and a second bump land formed at a prescribed region of the second surface thereof;

the conductive connectors each comprise a conductive bump; and

the conductive bumps are fused to respective ones of the first and second bump lands of each of the leads.

7. (Original) The semiconductor package of Claim 6 wherein each of the leads includes:

a first protective layer formed on at least a portion of the first surface thereof other than for the prescribed region including the first bump land; and

a second protective layer formed on at least a portion of the second surface thereof other than for the prescribed region including the second bump land.

8. (Original) The semiconductor package of Claim 7 wherein the protective layer is selected from the group consisting of:

a polyimide;

titanium;

aluminum; and

a solder resist.

9. (Original) The semiconductor package of Claim 1 wherein each of the leads includes:

a first protective layer coated on the first surface thereof about a respective one of the conductive connectors; and

a second protective layer coated on the second surface thereof about a respective one of the conductive connectors.

10. (Original) The semiconductor package of Claim 9 wherein the protective layer is selected from the group consisting of:

a polyimide;

titanium;

aluminum; and

a solder resist.

11. (Original) The semiconductor package of Claim 1 wherein the first and second semiconductor dies are identically sized.

12. (Original) The semiconductor package of Claim 1 wherein the encapsulating portion is applied to the leads such that the third surface of each of the leads is exposed within the encapsulating portion.

13. (Original) The semiconductor package of Claim 12 wherein the encapsulating portion is applied to the first and second semiconductor dies such that the bottom surface of the first semiconductor die and the top surface of the second semiconductor die are each exposed within the encapsulating portion.

14. (Previously Presented) The semiconductor package of Claim 13 wherein the leads and the first semiconductor die are oriented relative to each other such that the bottom surface of the first semiconductor die is substantially flush with the third surface of each of the leads.

15. (Currently Amended) The semiconductor package of Claim **[[12]]** **1** wherein:

each of the leads further defines an outer end which extends between the second and third surfaces thereof; and

the encapsulating portion is applied to the leads such that the outer end of each of the leads is exposed within the encapsulating portion.

16. (Original) The semiconductor package of Claim 1 wherein each of the leads further defines a fourth surface disposed in opposed relation to the third surface and laterally offset outwardly relative to the second surface.

17. (Original) The semiconductor package of Claim 16 wherein the encapsulating portion is applied to the leads such that the third and fourth surfaces of each of the leads are exposed within the encapsulating portion.

18. (Original) The semiconductor package of Claim 17 wherein the encapsulating portion is applied to the first and second semiconductor dies such that the bottom surface of the first semiconductor die and the top surface of the second semiconductor die are each exposed within the encapsulating portion.

19. (Original) The semiconductor package of Claim 18 wherein the second semiconductor die and the leads are oriented relative to each other such that the top surface of the second semiconductor die is substantially flush with the fourth surface of each of the leads.

20. (Original) The semiconductor package of Claim 19 wherein the first semiconductor die and the leads are oriented relative to each other such that the bottom surface of the first semiconductor die is substantially flush with the third surface of each of the leads.

21. (Original) The semiconductor package of Claim 17 further in combination with a second semiconductor package identically configured to the semiconductor package, the third surfaces of the leads of the second semiconductor package being electrically connected to respective ones of the fourth surfaces of the leads of the semiconductor package.

22. (Cancelled)

23. (Cancelled)

24. (Cancelled)

25. (Cancelled)

26. (Cancelled)

27. (Currently Amended) A semiconductor package comprising:

a plurality of leads;

a plurality of protective layers ~~disposed~~ **formed** on **prescribed regions of** respective ones of the leads, each of the protective layers**, at the time of formation,** being configured such that a portion of a corresponding one of the leads is exposed therein so as to define a land;

first and second semiconductor dies electrically and mechanically connected to the leads in opposed relation to each other through the use of a plurality of conductive connectors which abut respective ones of the lands; and

an encapsulating portion applied to and at least partially encapsulating the leads, the first and second semiconductor dies, and the conductive connectors such that portions of the leads are exposed in a common exterior surface of the encapsulating portion.

28. (Previously Presented) The semiconductor package of Claim 27 wherein a portion of one of the first and second semiconductors dies is exposed in the exterior surface of the encapsulating portion.

29. (Previously Amended) The semiconductor package of Claim 28 wherein the encapsulating portion defines an opposed pair of exterior surfaces, and portions of the first and second semiconductor dies are exposed in respective ones of the exterior surfaces.

30. (Currently Amended) A semiconductor package comprising:

a plurality of leads;

a plurality of protective layers ~~disposed~~ **formed** on **prescribed regions of** respective ones of the leads, each of the protective layers**, at the time of formation,** being configured such that a portion of a corresponding one of the leads is exposed therein so as to define a land;

first and second semiconductor dies electrically and mechanically connected to the leads in opposed relation to each other through the use of a plurality of conductive connectors which abut respective ones of the lands; and

an encapsulating portion applied to and at least partially encapsulating the leads, the first and second semiconductor dies, and the conductive connectors such that portions of each of the leads are exposed in respective ones of an opposed pair of exterior surfaces of the encapsulating portion.

31. (Previously Presented) The semiconductor package of Claim 29 further in combination with a second semiconductor package identically configured to the semiconductor package, at least some of the leads of the second semiconductor package being electrically connected to at least some of the leads of the semiconductor package.

32. (New) The semiconductor package of Claim 16 further in combination with a second semiconductor package identically configured to the semiconductor package,

at least some of the leads of the second semiconductor package being electrically connected to at least some of the leads of the semiconductor package.